Fabrication of an Organic Field-effect Transistor on a Mica Gate Dielectric

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We fabricated pentacene-based organic field-effect transistors (OFETs) using single-crystalline natural mica substrates as the gate dielectric. Substrate temperatures during the deposition of pentacene films were varied from room temperature (RT) to 90 °C. Epitaxial growth of the pentacene film on the mica surface was observed even at RT. The FET working characteristics on the mica gate dielectric have been observed for the first time.

Recently, OFET has been widely studied and its device performance has been considerably improved.[1] In many studies of OFET, thermally grown SiO_x on a conductive Si substrate has been used as the gate dielectric, but the use of SiO_x sometimes limits the performance of OFET. For instance, the dielectric constant of SiO_x is rather low ($\varepsilon \approx 4$), which requires high operation voltage. To overcome this difficulty, many groups have studied high dielectric constant materials instead of SiO_x.[2–5] Another disadvantage to use SiO_x is its crystallinity, because a single-crystalline organic film could not grow on the amorphous SiO_x. The initial organic layer on the gate substrate mainly rules the working characteristics of OFETs.[6,7] Thus, the improvement of the crystallinity at the organic-gate dielectric interface is expected to decrease defects or grain boundaries, resulting in enhancement of the OFET performance.

In the present work, we tried to fabricate OFETs on layered material substrates. When an organic film is grown on a cleaved surface of the single-crystalline layered material, the crystallinity of the grown film is improved and its defects are reduced. Indeed, successful epitaxial growth of organic films on layered material substrates such as MoS_2, mica, GeS, etc., have been reported.[8–12] Here, we focus on "muscovite mica" as the gate dielectric of OFETs. Mica is less expensive than SiO_x, and its cleaved surface has excellent flatness and crystallinity. Mica has been used as a capacitor or an insulator in electric circuits for a long time. To our knowledge, however, mica was not utilized as the gate dielectric in OFETs so far. Thus, we tried to fabricate OFETs on mica gate substrates by depositing epitaxial films of pentacene, which is the most popular organic semiconductor for OFETs. We investigated the growth mechanism of pentacene films grown at different substrate temperatures, and evaluated the field-effect mobility by measuring the conductivity for various gate voltages.

A natural mica (muscovite) substrate was cleaved using an adhesive tape in atmosphere to approximately 1 µm thick and used as the gate substrate without further surface treatment. The gate electrode of Au was thermally deposited onto the backside of the mica substrate. As-purchased pentacene (98%, Aldrich Chem. Co.) was evaporated from a Knudsen cell onto the mica surface for 2 h under the ultrahigh-vacuum condition (ca. 10^{-7} Pa). The deposition rate was maintained at 1.2 nm·min^{-1} and the substrate temperature was set at RT, 60 or 90 °C. The nominal thickness of the pentacene film was measured by a crystal quartz thickness monitor. Finally, source and drain electrodes of Au were formed by thermal deposition through a metal shadow mask placed on the pentacene film. The channel length (L) and width (W) in the top-contact OFET were 0.1 and 1.0 mm, respectively. Working characteristics of OFETs were measured in a vacuum desiccator (ca. 1 Pa). The morphology and the crystallinity of pentacene films on mica surfaces were investigated by atomic force microscopy (AFM), X-ray diffraction (XRD) and reflection high-energy electron diffraction (RHEED).

Figure 1 shows the AFM images of pentacene films grown on the mica surfaces for various substrate temperatures and deposition times. In the case of pentacene films deposited for 15 min, flat and wide domains appeared only at increased substrate temperatures. The pentacene films deposited at 60 and 90 °C were better ordered than at RT. A similar result was found for the pentacene films grown on hydrogen-terminated Si(111) surfaces.[13] When pentacene was deposited for 2 h, domains became larger along with increasing the substrate temperature. At 90 °C, however, amount of the pentacene molecules on the substrate was smaller than at RT or 60 °C owing to the re-evaporation. Thus, the thickness of the grown film was thinner, and gaps among domains were wider. It was difficult to grow an enough thick pentacene film at 90 °C in a reasonable deposition time.

Figure 2 shows XRD patterns of the pentacene films deposited on mica for various substrate temperatures. The XRD peaks from the pentacene films were labeled as (001) and (002), and indicated by dotted lines. Other large reflection peaks come from the mica substrate. According to the XRD patterns, the pentacene film deposited at RT consisted of a single phase, so called "thin-film" one that has the layer spacing of 1.53 nm. When the substrate temperature was raised to 60 °C, the pentacene film

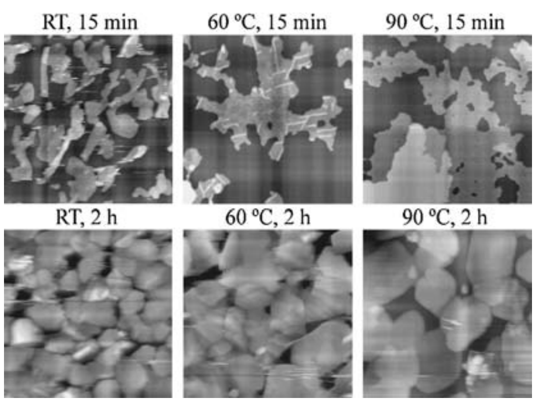

Figure 1. AFM images of pentacene films grown on the mica surfaces for various substrate temperatures and deposition times. All images show $2 \times 2\,\mu m^2$ scan area.

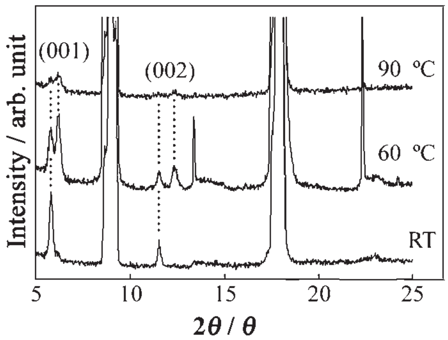

Figure 2. XRD patterns of pentacene films deposited on the mica surfaces at various substrate temperatures.

consisted of a mixture of two phases, "thin-film" and "bulk" phases.[14] The latter corresponds to the layer spacing of 1.42 nm. In the case where the substrate temperature was 90 °C, the pentacene film mainly consisted of the "bulk" phase. But every peak was smaller than RT or 60 °C because of the thinner film thickness.

To investigate the crystal structure of pentacene films on the mica surfaces, we carried out RHEED measurement. After the growth of pentacene films with 0.6–1.2 nm thickness, the streak patterns coming from the mica substrates became dim. Thereafter, new streaks together with spots appeared for the films thicker than about 1.5 nm. These patterns were kept unchanged after the multilayer growth of pentacene. Similar streak patterns were observed for all substrate temperatures. When pentacene was deposited on a thermally grown SiO_x, no streak pattern was observed. Therefore, the in-plane ordering of the pentacene film grown on the mica surface is supposed to be better than that on thermally grown SiO_x.

Figure 3 shows the drain–source current (I_D) versus drain–source voltage (V_D) characteristics of the pentacene OFET fabricated on mica at 60 °C for the various gate–source voltage (V_G). Gate leak current was smaller than 1 nA even for the elevated gate voltage. The field-effect mobility (μ) was evaluated in the linear region using a following equation:

$$\frac{\partial I_D}{\partial V_G} = \frac{WC\mu}{L} V_D, \quad (1)$$

where C is the capacitance per unit area of the gate dielectric; 3.5 $nF{\cdot}cm^{-2}$ for 1 µm thickness mica. On the mica gate, μ was $2.4 \times 10^{-3}\,cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ for the film grown at 60 °C, while μ for the films grown at RT and 90 °C were $4.6 \times 10^{-4}\,cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ and $2.6 \times 10^{-4}\,cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, respectively. The on–off ratio and the threshold voltage (V_{th}) were best for the film grown at 60 °C, and they were 11 and 88 V, respectively. In the case of OFET fabricated at RT, the pentacene film had smaller domains and more grain boundaries, and the film crystallinity was poor. The pentacene film grown at 90 °C was too thin to show good OFET performance.

The mobility, on–off ratio and V_{th} of the pentacene OFET fabricated on the mica gate substrate were much worse than those on amorphous SiO_x.[1] We ascribe its poor performance to following reasons. First, the cleavage of mica might be incomplete so that its surface was rather rough, or some small irregular pieces of cleaved flakes remained between source and drain electrodes. Usually, a narrow area of the cleaved mica surface is atomically smooth, but some defects or steps can exist in the

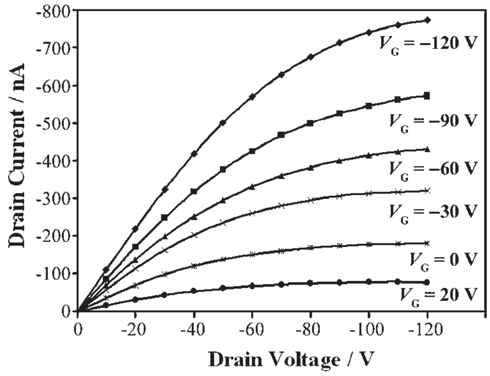

Figure 3. Drain–source current (I_D) versus drain–source voltage (V_D) characteristics of pentacene OFET fabricated on mica at 60 °C for various gate–source voltage (V_G).

wider channel region of OFET. Next, the Au gate electrode deposited on the backside of the mica substrate might be poorly attached to mica because of the inertness of the mica surface. In this case, injection of hole carriers into the pentacene layer will be reduced. These problems should be technically improved, which are currently under investigation. Another possibility is that randomly distributed potassium ions on the cleaved surface of mica might work as a positively charged scattering center for holes in the channel. This problem could be overcome by using another kind of layered silicate without cations on its cleaved surface.

In summary, we explored possibility of fabrication of OFETs on *inexpensive* and *single-crystalline* natural mica substrates. By observing the morphology and the ordering of pentacene films on the mica surfaces by XRD, AFM, and RHEED, epitaxial growth of pentacene was confirmed. Typical FET characteristics were observed for the pentacene OFET on the mica gate dielectric although the mobility at the present stage was still low as compared with that on SiO_x.

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